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September 10, 2003

Dr. Michael Witherell, Director
Fermilab National Accelerator Laboratory

Dear Dr. Witherell,

We are pleased to present the attached preliminary proposal for a Layer-0 Silicon Detector. The detector represents a very attractive addition to the DZero experiment since it will ensure efficient tracking as radiation damage, sensor and readout attrition, and increased instantaneous luminosity all lessen the capabilities of the current silicon detector. The improved tracking and b-tagging will greatly strengthen the search potential of DZero and the entire Run II program.

The sub-project will benefit considerably from previous Run IIb silicon R&D and material procurement. The first studies also indicate the device can be installed during the scheduled summer 2006 shutdown. Nonetheless, there are a number of issues that require further study. We therefore request an early indication of your support and encouragement to pursue this sub-project, along with the more specific go-ahead to pursue the detailed studies that will be needed to bring the project into focus over the next few months.

Sincerely,

Gerald C. Blazey
Co-Spokesperson

John Womersley
Co-Spokesperson

Jonathan Kotcher
Run IIb Project Manager

September 10, 2003
Version 1.2

Initial Proposal for a Layer 0 Silicon Detector for the DØ Experiment

Introduction

The performance of the DØ tracking system will degrade over the course of Run II. Causes of diminished performance include radiation damage, micro-discharge effects, failure of individual detector components and radiation incidents. In addition increased instantaneous luminosity will increase occupancy in the inner CFT layers, making the tracking more dependent on the silicon system. Given operating experience to date, it is possible that a minority of the barrel silicon will be operational at the end of 2006. To not only preserve but also enhance the physics capabilities of the Run IIa silicon detector we propose to build a new, single layer, inner silicon detector with carbon fiber support and integrated cooling, which can be installed inside the current Run IIa SMT in the collision hall during the anticipated shutdown of the Tevatron in the year 2006. The conceptual design of the detector is described in this letter. Many of the details of the design still need careful study. Certain aspects of the design described here are therefore, by necessity, vague.

Design

The proposed detector will have a carbon fiber support structure analogous to the support structure originally designed for the inner layers of the Run IIb detector. It has a crenellated geometry with 6-fold symmetry. There are two sublayers denoted as layer 0A and 0B. The support structure will consist of two elements (see Figure 1); a twelve sided backbone tube with anticipated four layer $[0,90]_s$ lay-up, and a crenellated structure expected to have six layers with $[0,20,-20]_s$ lay-up. A prototype support cylinder with identical lay-up, albeit with larger inner diameter, was successfully built for the proposed Run IIb detector. The detector would be supported on the beam pipe.

The Layer 1A HDI components on the current Run IIa silicon detector determine the limiting aperture within which the new detector elements could be installed. A preliminary investigation of a possible layout indicates that silicon radii of approximately 15.8 mm and 20.2 mm are feasible for layers 0A and 0B, respectively. The sensors for layer 0B can be two-chip wide. It is expected that the sensor design already developed for the Run IIb detector can be adopted for the sensors for layer 0B. These sensors have 50 μm pitch with intermediate strips. Retaining a pitch of 50 μm for Layer 0A would result in a sensor with 168 strips. Alternatively, one could opt for a one-chip wide sensor with a strip pitch of 62.5μm with intermediate strips. Sensors will be 80mm long, with twelve sensors longitudinally per phi-segment. Figure 2 shows a cross section of the proposed layer 0 detector embedded in the current Run IIa silicon detector.

Figure 3 shows the expected improvement on the impact parameter resolution from the addition of a Layer 0 detector. In this simulation the Layer 0 sensors were assumed to have a pitch of 25 μm without intermediate strips. The radial position of Layer 0A was at 15.6 mm and Layer 0B at 18.4 mm. For tracks with low transverse momentum an improvement of a factor of two in impact parameter resolution can be obtained by the addition of an extra layer close to the beamline. Also the pattern recognition for tack reconstruction will benefit from the information provided by the additional layer.

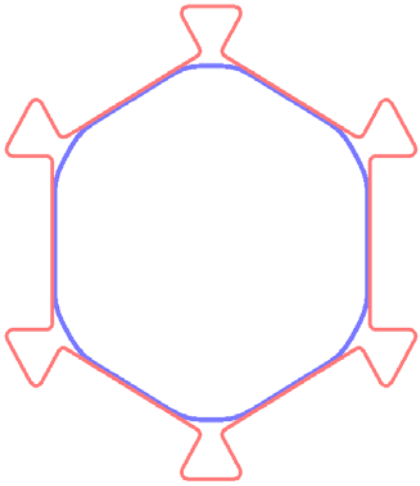

Figure 1: Cross section of the Run IIb Layer 0 sensor support structure

The sensors will be read out with analogue cables connected to hybrids outside the tracking volume. Although these cables are technically challenging, we have completed a very successful prototyping effort of these cables for the Run IIb detector. The last set of 40 prototype cables we received was flawless and demonstrates the capability of the vendor to produce cables to our specifications. We expect to carry the design for the Run IIb analogue cables over to the Layer 0 detector design. Figure 4 shows a picture of a prototype Layer 0 assembly for the Run IIb detector with the analogue cable on the left, mounted onto the hybrid with two SVX4 chips, and the digital jumper cable on the right. To reduce the load capacitance on the readout chips, the lengths of the analogue cables will be minimized. Details regarding the locations of the hybrid support structures need to be determined

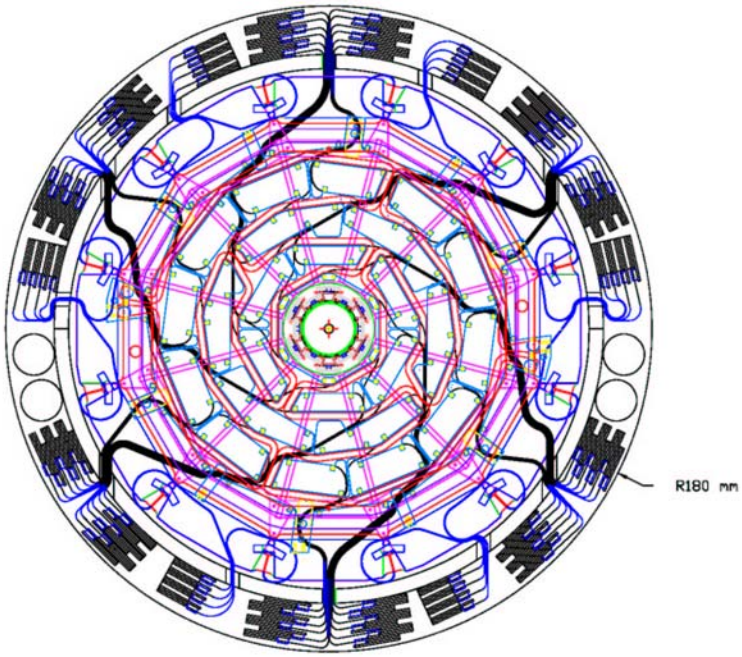

Figure 2: Cross section of the proposed Layer 0 detector inside the current Run IIa silicon detector.

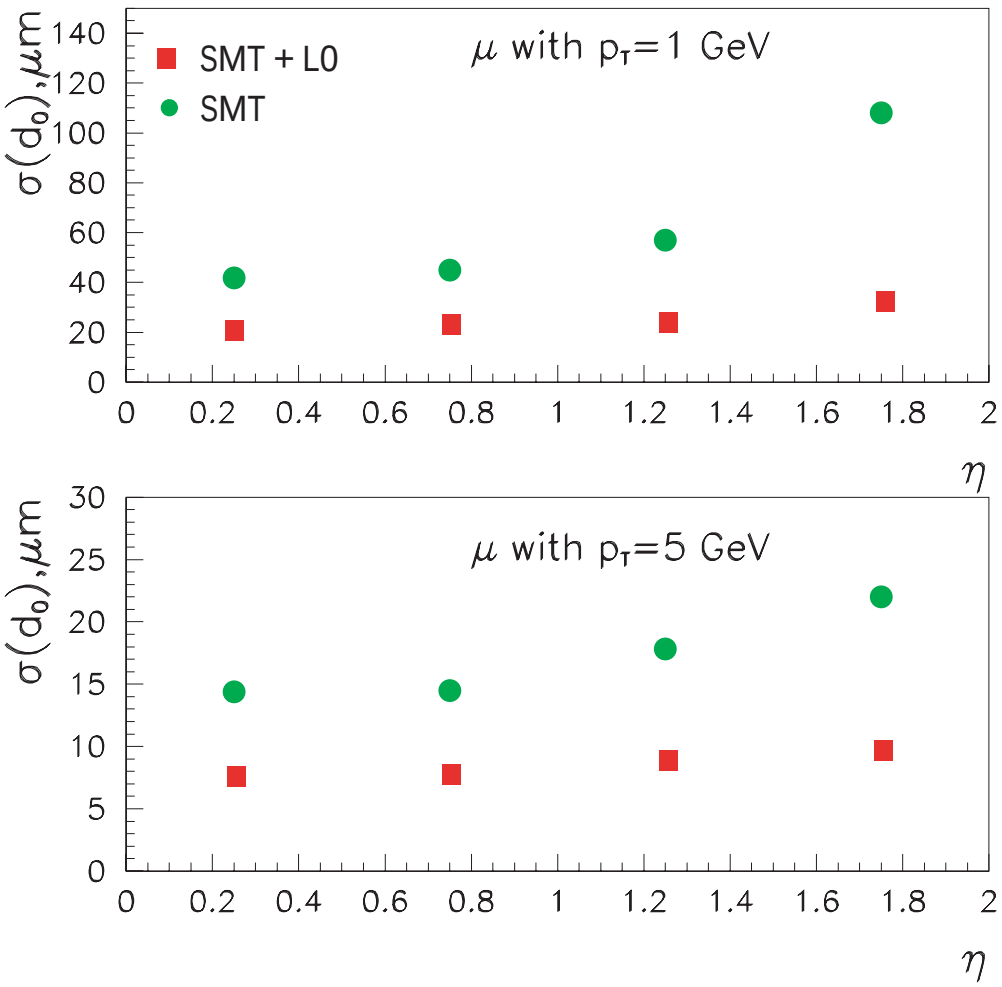

Figure 3: Expected improvement in impact parameter resolution with a Layer 0 detector added to the current Run IIa silicon detector.

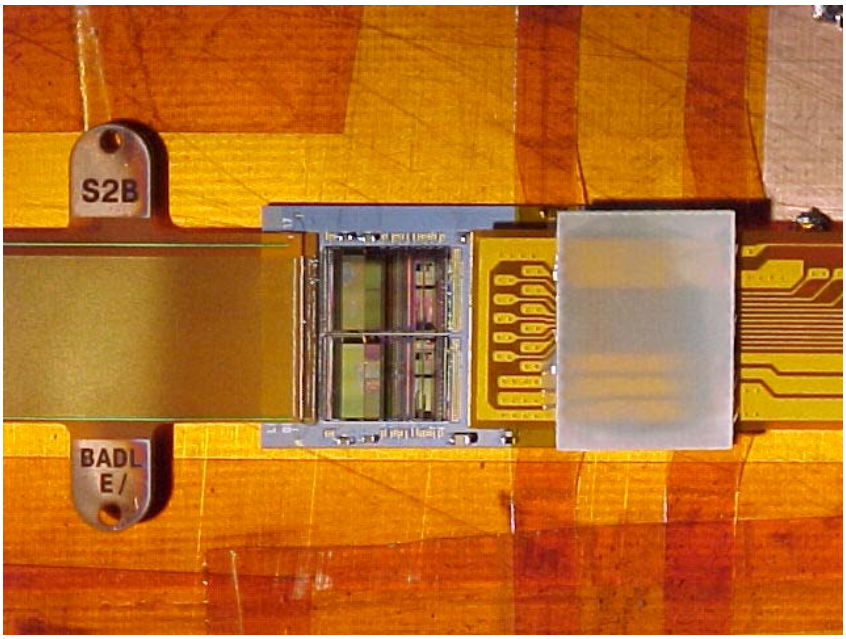

Figure 4: Assembly of prototype analogue cable, hybrid and digital jumper cable for the innermost layer for the Run IIb detector.

Readout

There are two options for the readout of the layer 0 sensors. One possibility is to employ SVX2 chips to readout the sensors. The current system employs readout with the SVX2 chip. The experiment has 15 wafers of SVX2 chips available, though those wafers are currently untested. These wafers should provide enough readout chips for a Layer 0 detector. The infrastructure to readout the SVX2 chips is already in place in the experiment, but the hybrids and low mass cables would need to be designed. It should also be noted that both at SiDet and at DØ there are still test setups available to readout modules with SVX2 chips, which can be converted into burn-in test stands. Alternatively, the new detector can be readout with the SVX4 chip. There are 24 wafers of the latest version of the SVX4 chip available, which should yield about 7500 chips. We foresee 72 one-chip wide sensors and 72 two-chip wide sensors, so only 216 readout chips are needed. Using the SVX4 readout chip, all the development for the Run IIb detector can be retained. The hybrids for Layer 0 have been designed and prototype hybrids have been received. The design for the digital cable, junction cards and adapter cards can be carried over. The SVX4 is expected to be more robust and have better performance than the SVX2.

Adequate grounding of the detector to minimize noise pickup is of utmost importance. We have a completely designed and partially tested grounding scheme developed for the Run IIb inner detector. We expect to fully test and certify a full prototype Run IIb inner detector using this grounding scheme. We anticipate that this grounding scheme should be directly applicable to the Layer 0 design.

The high voltage power supplies for the complete Run IIb detector have been purchased using funds from Cinvestav, Mexico. Two Wiener power supplies for the low voltage have also been purchased and could be used to provide the power for the SVX4 chips. The current 80-conductor cables and Interface Boards are only rated up to a voltage of 300V. A careful re-evaluation has to be performed to understand the time evolution of the depletion voltage for the innermost sensors of Layer 0, given the recently revised anticipated luminosity profile, to determine if bias voltages in excess of 300 Volts are needed.

A total of 36 80-conductor cables each are needed in the north and south horseshoe area to interface the Layer 0 detector with the existing readout system. These cables could be provided by sacrificing part of the H-disk readout. The H-disks currently use 96 80-conductor cables. Using the cables of the H-disks has the additional advantage that these cables are nicely mapped onto sequencer and VRB slots, which would greatly facilitate incorporating the Layer 0 detector into the silicon vertex trigger.

Installation

Details of the installation are preliminary, but a plausible plan is to install the new silicon by passing it through the beam pipe opening of one End Calorimeter. The same approach would be used first to remove the Run IIa beam pipe. The beam pipe through the end calorimeter has an OD = 50.8 mm and an ID = 48.463 mm. It passes through an opening of approximately 57.836 mm diameter. A possible plan is to remove the EC beam tube to obtain the maximum available diameter (~ 57.8 mm) for silicon installation via the EC opening. Cutting the pipe to remove it and re-welding it after silicon installation appears to work. In addition, the shielding outside the EC needs to be opened for access.

New cable installations for both readout schemes, SVX2 and SVX4, have been considered. For the SVX2 scenario, low voltage will be delivered with the infrastructure already in place. For the SVX4 scenario, a minimal number of cables will need to be installed along with the new power supply system already in hand. Routing paths for high voltage and low voltage have already been determined. Cabling of the new detector to the adapter cards on the horseshoe ring is very straightforward. All adapter cards are located on the outermost ring, therefore minimizing the number of cable disconnects necessary to complete the installation of the Layer 0 detector.

Cost

A very rough estimate of the cost has been obtained through comparison with the cost for the Run IIb Layer 0 detector. Some cost estimates for the Run IIb detector have been updated since more reliable information is now available. The upper part of Table 1 indicates the anticipated cost for the new device. The lower part of Table 1 lists the equipment already in hand and the savings associated with those items. Note that in some cases only a portion of the tabulated savings is realized since more parts were ordered than are needed for the Layer 0 detector. The savings for the SVX4 readout chip only

includes the cost of the two full chip MOSIS submissions. Engineering costs have been not been included. Extensive R&D is not foreseen for the new detector, since most of the groundwork has been laid already during the R&D phase of the Run IIb detector. Some design and detailed prototyping, however, will be necessary and is not included in Table 1 below. Amounts are in FY02 dollars and do not include labor, contingency, or G&A. We note that a large portion of the M&S cost might potentially be supported through MRI funds.

Item	Cost (k$)
Sensors	233
Hybrids	59
Analogue Cables	140
Digital and Twisted Pair Cables	60
Mechanical Structure	100
Fixturing	90
Downstream Electronics	100
Grounding Elements	45
Total	827

Existing Equipment	Cost (k$)
High Voltage Power Supplies	200
Low Voltage Power Supplies	16
SVX4 Readout Chips	371
Total	587

Table 1: Preliminary cost estimate (upper table) and cost savings (lower table) for a Layer 0 detector.

Schedule

Based upon the accumulated experience gained with the Run IIa detector, and the Run IIb detector through the prototyping phase, we anticipate that the detector described above represents a project which can be mounted within a two year time frame. The installation schedule is at this point a conjecture. We anticipate the following sequence of events. Although the tasks are listed serially, some of them might be done with greater parallelism.

Week 1: Open EC's, install access platforms, open shielding outside one EC, drain silicon coolant
Week 2: Un-cable and remove H-disks

Week 3: Remove pipes of one EC, bring new silicon to D0

Week 4: Install silicon (mechanically), connect cooling and dry gas lines, begin re-connecting and leak checking beam pipes

Week 5: Leak check and begin silicon coolant flow, complete beam pipe leak checking, begin cabling

Week 6: Cable and check readout

Week 7: Cable and check readout

Week 8: Enclose dry gas volumes, remove platforms, close EC's, close shielding